USP-186 – 80C186 Family In-Circuit Emulator

- 1 MB of Dual-Ported Memory
- Emulation Up to 64 MHz (Crystal)
- 3.3V and 5V Targets Support
- HLL Debugging for C/C++
- 32K by 80-Bit Selective Trace Buffer
- 32-Bit Time Stamp in Trace
- Complex Hardware Breakpoints and Passpoints
- Unlimited Address and Data Match Breakpoints
- Execution Coverage Monitor
- LAN Support for Remote Debugging

USP-186 offers real time in-circuit emulation, development and HLL debugging for the entire 80C186 family of chips.

USP-186 comes with full 1 MB of memory, C/C++ and ASM debugger, 80 bit wide by 32K deep trace buffer, and a sophisticated Event Triggering System that uses combinations of address and data comparators, sequencer, external probes, and pass counters to create almost any complex trigger condition.

The zero wait state, dual-ported memory allows the user full read/write access to the emulation memory, without slowing down the running processor. Because of this unique feature, watching and modifying the variables and parameters can be done without stopping the processor and disrupting the running application.

Selective tracing of only meaningful data is easily achieved with the aid of the event triggering system. A 32-bit time stamp records exact time relationships between instructions and routines in absolute or relative modes with a 100 nsec resolution.

The HLL debugger provides support for Intel, Microsoft, and Borland compilers. Unlimited number of breakpoints and passpoints may be set or cleared with a mouse, by simply clicking on the desired instruction in the source window. You can watch variables change on-the-fly, and
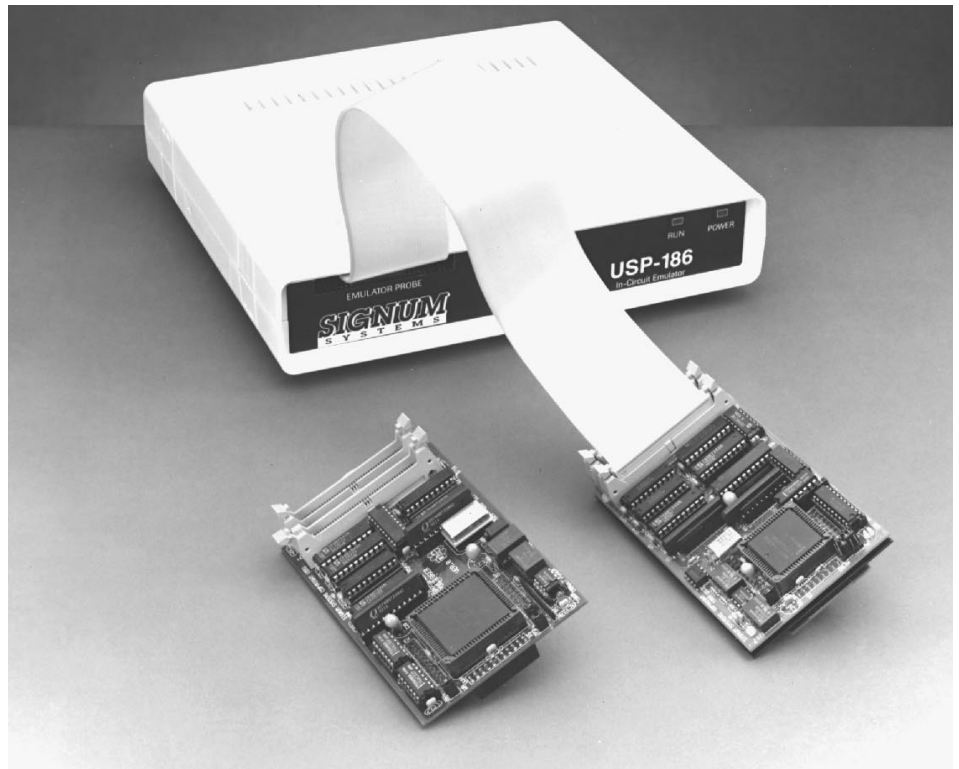
zoom in on any member of a complex structure with a click of a mouse.

A build-in hardware Coverage Monitor captures in real-time every program fetch, memory read/write, and I/O read/write transaction. Collecting these transactions may be done individually or in any combination of them to display a map of memory usage and help in finding code that never executes, variable usage, un-initialized memory reads, or illegal memory accesses.

The emulation CPU (either bondout or standard) is mounted on a probe assembly, which plugs directly into the target system, for fast and noise free emulation.

HOST SYSTEMS SUPPORTED:
IBM-386/486/Pentium® processors running MS-DOS* or MS-Windows* 95/NT

PROCESSORS SUPPORTED:
80186/188 @ 10 MHz, 5V
80C186XL/188XL @ 25 MHz, 5V
80C186EA/188EA @ 25 MHz, 5V
80C186EB/188EB @ 25 MHz, 5V
80L186EB/188EB @ 16 MHz, 3.3V
80C186EC/188EC @ 25 MHz, 5V
80L186EC/188EC @ 16 MHz, 3.3

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